REMARKS/ARGUMENTS

Claims 1-4, 6-13, 15-21 and 23-26 are pending in the present application. Claims 6, 15, and 23 were canceled; claims 1-4, 7-13, 16-21 and 24-26 were amended; and claims 27-29 were added. Support for these amendments may be found in the Specification at least on pages 20 through 22 and in Figures 3, 7, 8, and 15 and their accompanying text. No new matter has been added by any of the amendments Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation

The Office Action has rejected claim 26 under 35 U.S.C. § 102 as being anticipated by *Pardo et al.*, Apparatus and Method for Implementing Watchpoints and Breakpoints in a Data Processing System, U.S. Patent No. 5,754,839, May 19, 1998 (hereinafter "*Pardo*"). This rejection is respectfully traversed.

Regarding claim 26, the Office Action states:

> **Claim 26:**
> A method in a data processing system for monitoring the execution of a compiled program, the method comprising:
> receiving a bundle, wherein the bundle comprises a plurality of instructions and wherein the bundle is a multiple of 128 bits (see for example column 5, lines 51-66);
> identifying an instruction out of the plurality of instructions in the bundle (see for example column 5, lines 51-66);
> determining whether the instruction has an associated performance indicator (see for example column 5, lines 51-66) ;
> responsive to a determination that a performance indicator is associated with the instruction, transmitting a signal to a performance monitor (see for example column 6, lines 1-14); and
> processing the instruction (see for example column 6, lines 1-14).

Office Action dated August 23, 2007, pp. 2-3 (emphasis in original).

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Amended independent claim 26 recites:

26. A computer implemented method in a data processing system for monitoring the execution of a compiled program having a set of groupings, the computer implemented method comprising:

selecting a grouping from the set of groupings for the compiled program to form a selected grouping;

determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data for determining a performance efficiency on an execution of the instruction by a processor executing the instruction is to be generated;

responsive to the determining that the indicator is present, sending a signal to a performance monitor;

generating, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction, responsive to the indicator being present during execution of the compiled program;

storing, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction;

determining the performance efficiency on the execution of the instruction, to form a determined performance efficiency; and

reporting the determined performance efficiency to a user.

Pardo fails to anticipate claim 26, as *Pardo* fails to teach each and every feature of amended independent claim 26. Specifically, *Pardo* fails to teach the features of (1) determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data for determining a performance efficiency on an execution of the instruction by a processor executing the instruction is to be generated; (2)responsive to the determining that the indicator is present, sending a signal to a performance monitor; (3)generating, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction responsive to the indicator being present during execution of the compiled program; (4) storing, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction; and (5) determining the performance efficiency on the execution of the instruction, to form a determined performance efficiency.

Pardo, in column 5, lines 50-63, teaches setting watchpoints, which monitors a specific address. When an instruction is fetched, a watchpoint indicator is generated by an I-bus support logic. Thus, the indicator, the watchpoint indicator, taught by *Pardo* is not part of the instruction as recited in claim 26. Rather, as taught by *Pardo*, the watchpoint indicator is generated after the instruction is received initially. In particular, the indicator is generated when an already received instruction is fetched from a particular address. Thus, *Pardo* fails to teach the feature of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein

the indicator indicates that data for determining a performance efficiency on the execution of the instruction by a processor executing the instruction is to be generated." Therefore, *Pardo* fails to anticipate claim 26 of the present invention.

Furthermore, as recited in claim 26, "the indicator indicates that data for determining a performance efficiency on the execution of the instruction by a processor executing the instruction is to be generated." In contradistinction, *Pardo* teaches that the watchpoint indicator merely causes a counter to be decremented when the watchpoint is moved to a history buffer and the watchpoint's associated instruction is issued to an execution unit. Thus, *Pardo* allows for the counting of the execution of instructions that were stored in particular address locations. Therefore, *Pardo* fails to teach, "the indicator indicates that data for determining a performance efficiency on the execution of the instruction by a processor executing the instruction is to be generated." Thus, *Pardo* fails to teach the feature of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data for determining a performance efficiency on the execution of the instruction by a processor executing the instruction is to be generated." Therefore, *Pardo* fails to anticipate claim 26 of the present invention.

Additionally, in column 6, lines 1-4, *Pardo* teaches that when an instruction is issued to an execution unit, a counter module decrements a count. The count is then sent to a history buffer. The watchpoint indicator is also sent to the history buffer. Thus, the data generated by *Pardo*, a count, is not the same as the data recited in claim 26, "data for determining a performance efficiency on the execution of the instruction by a processor executing the instruction." Even assuming *arguendo* that the data taught by *Pardo* is equivalent to the data recited in claim 26, *Pardo* still fails to teach claim 26. Claim 26 recites the features of "responsive to a determination that an indicator is present, sending a signal to a performance monitor; generating, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction responsive to an indicator being present during execution of the compiled program; and storing, by the performance monitor, the data for determining the performance efficiency on the execution of the instruction." Figure 2 of *Pardo* clearly shows that the counter module and the history buffer are two distinct, separately functioning, independent, physical units. Thus, *Pardo* cannot teach sending a signal to a performance monitor, generating the data by a performance monitor, and storing the generated data by the performance monitor as *Pardo* teaches that the generating and storing are performed by two distinct, separately functioning, independent, physical units.

Additionally, *Pardo* fails to teach the feature of "determining the performance efficiency on the execution of the instruction, to form a determined performance efficiency." Nowhere does *Pardo* mention determining a performance efficiency.

Therefore, for at least the reasons set forth above, Applicants submit that *Pardo* fails to anticipate 26, as *Pardo* fails to teach each and every feature of claim 26. Thus, Applicants submit that claim 26 is in condition for allowance over the *Pardo* reference.

Therefore, the rejection of claim 26 under 35 U.S.C. § 102 has been overcome.

II. 35 U.S.C. § 103, Obviousness

The Office Action has rejected claims 1-4, 6-13, 15-21, and 23-25 under 35 U.S.C. § 103 as being unpatentable over *Kaneshiro et al.*, Profile Instrumentation Method and Profile Data Collection Method, U.S. Patent No. 5,950,003, September 7, 1999 (hereinafter "*Kaneshiro*") in view of *Pardo*. This rejection is respectfully traversed.

Regarding claim 1, the Office Action states:

> **Claim 1:**
> *Kaneshiro* discloses a method in a data processing system for monitoring the execution a compiled program having a set of groupings, the method comprising:
> selecting a grouping from the set of groupings (see for example column 8, lines 7-17) for the compiled program to form a selected grouping (see for example);
> associating a set of indicators with instructions in the selected grouping within the set of groupings, wherein theset of indicators provides data on the execution of the instructions by a processor executing the instructions (see for example column 13, lines 15-43); and
> collecting the data (see for example column 7, line 65- column 8, line 7). However, *Kaneshiro* does not disclose a method in a data processing system for monitoring the execution a compiled program having a set of groupings comprising: ,
> executing the compiled program, wherein data is generated in response to a determination that an instruction of the instructions is associated .with an indicator in the set of indicators, the data comprising at least one of a number of times each instruction on the selected grouping has been executed and a number of visits to the selected grouping.
> *Pardo* in the same analogous art of profiling in data processing systems discloses a method in a data processing system for monitoring the execution a compiled program having a set of groupings comprising:
> executing the compiled program, wherein data is generated in response to a determination that an instruction of the instructions is associated with an indicator in the set of indicators, the data comprising at least one of a number of times each instruction on the selected grouping has been executed and a number of visits to the selected grouping (see for example column 2, lines 7-29, and 44-45). Therefore at the time of the invention it would have been obvious to a person of ordinary skill in the art to utilize the feature disclosed in *Pardo* to enhance the profiling method taught in *Kaneshiro* (see for example *Pardo*, column 1, lines 60-63).

Office Action dated August 23, 2007 (emphasis in original).

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The prior art reference (or references when combined) must

teach or suggest all the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In determining obviousness, the scope and content of the prior art are... determined; differences between the prior art and the claims at issue are... ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or non-obviousness of the subject matter is determined. *Graham v. John Deere Co.*, 383 U.S. 1 (1966). "Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l. Co. v. Teleflex, Inc.*, No. 04-1350 (U.S. Apr. 30, 2007). "*Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.* Id. (citing *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006))."

Amended independent claim 1, which is representative of amended independent claims 10 and 18 with regards to similarly recited subject matter, recites:

> 1. (Currently Amended) A computer implemented method in a data processing system for monitoring the execution of a compiled program having a set of groupings, the computer implemented method comprising:
> selecting a grouping from the set of groupings for the compiled program to form a selected grouping;
> determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data on an execution of the instruction by a processor executing the instruction is to be generated;
> responsive to the determining that the indicator is present, sending a signal to a performance monitor;
> generating the data on the execution of the instruction responsive to the indicator being present during execution of the compiled program; and
> storing the data on the execution of the instruction.

The Examiner has failed to state a *prima facie* obviousness rejection against claim 1 because the proposed combination of the references, when considered as a whole, does not teach all of the features of claim 1. Specifically, the proposed combination, considered as a whole, does not teach the features of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data on the execution of the instruction by a processor executing the instruction is to be generated."

Kaneshiro, in column 13, lines 15-43, teaches that when instructions are inserted into loops, library calls for counting and clocking loop iterations need to be inserted as well. Thus, *Kaneshiro* fails to teach, "determining, for each instruction in the selected grouping, whether an indicator is present" and

"wherein the indicator is a portion of the instruction." Therefore, *Kaneshiro* fails to teach the feature of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data on an execution of the instruction by a processor executing the instruction is to be generated." *Kaneshiro* does not suggest, "determining, for each instruction in the selected grouping, whether an indicator is present" because *Kaneshiro* teaches that, in response to instructions being inserted into a loop, library calls are automatically inserted into the loop is well. Therefore, there is no reason to make a determination, as taught by *Kaneshiro*. Additionally, as library calls are clearly separate from the inserted instruction, clearly the library calls are not a portion of the instruction. Therefore, *Kaneshiro* also fails to suggest, "wherein the indicator is a portion of the instruction."

Additionally, *Pardo*, in column 5, lines 50-63, teaches setting watchpoints, which monitors a specific address. When an instruction is fetched, a watchpoint indicator is generated by an I-bus support logic. Thus, the indicator, the watchpoint indicator, taught by *Pardo* is not part of the instruction as recited in claim 1. Rather, as taught in *Pardo*, the watchpoint indicator is generated separate from the instructions, after the instruction is received initially. In particular, the indicator is generated when an already received instruction is fetched from a particular address. Then the watchpoint is stored along with the instruction that gave rise to the wathcpoint in the instruction queue. (See *Pardo*, column 5, lines 64 – 66) Thus, *Pardo* fails to teach or suggest the feature of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data on an execution of the instruction by a processor executing the instruction is to be generated."

Thus, the combination of *Kaneshiro* in view of *Pardo* fails to teach or suggest the feature of "determining, for each instruction in the selected grouping, whether an indicator is present, wherein the indicator is a portion of the instruction and wherein the indicator indicates that data on an execution of the instruction by a processor executing the instruction is to be generated." Thus, the proposed combination of *Kaneshiro* in view of *Pardo* fails to render obvious claim 1. Furthermore, as amended independent claim 1 is representative of amended independent claims 10 and 18, the same distinctions between the combination *Kaneshiro* in view of *Pardo* and the claimed invention in claim 1 applies to amended independent claims 10 and 18. Therefore, Applicants submit that claims 1, 10, and 18 are in condition for allowance over the proposed combination of *Kaneshiro* in view of *Pardo*. Claims 2-4, 7-9, 11, 12, 16, 17, 19-21, 24, 25 and 27-29 depend from claims 1, 10, and 18. Thus, Applicants submit that claims 2-4, 7-9, 11, 12, 16, 17, 19-21, 24, 25 and 27-29 are also in condition for allowance, at least by virtue of their

depending from an allowable claim. Additionally, at least claims 27-29 claim other additional combinations of features not suggested by the references. Consequently, it is respectfully urged that the rejection of claims 1-4, 6-13, 15-21, and 23-25 have been overcome.

Therefore, the rejection of claims 1-4, 6-13, 15-21, and 23-25 under 35 U.S.C. § 103 has been overcome.

III. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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